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Pulsed Capacitance Measurement of Silicon Carbide (SiC) Schottky Diode and SiC Metal Oxide Semiconductor

by Timothy E. Griffin

ARL-TR-3993 **November 2006**

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
November 2006	Final	March to May 2006

4. TITLE AND SUBTITLE
Pulsed Capacitance Measurement of Silicon Carbide (SiC) Schottky Diode and SiC Metal Oxide Semiconductor

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Timothy E. Griffin

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
U.S. Army Research Laboratory
ATTN: AMSRD-ARL-SE-DP
2800 Powder Mill Road
Adelphi, MD 20783-1197

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TR-3993

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U.S. Army Research Laboratory
2800 Powder Mill Road
Adelphi, MD 20783-1197

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The incremental capacitance *C* was measured for a silicon carbide (SiC) Schottky diode during a reverse-biasing pulse and for two SiC n-MOS transistors during a negative pulse to their source with the drain grounded. *C* was measured as a function of pulsed voltage to 600 V, and on a gain-phase analyzer as a function of frequency and bias voltage to 40 V.

15. SUBJECT TERMS
Pulsed capacitance measurement, SiC diode, MOS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE	SAR	30	Timothy E. Griffin
Unclassified	Unclassified	Unclassified			19b. TELEPHONE NUMBER (*Include area code*) 301-394-5523

Contents

List of Figures

List of Tables

1. Introduction

Developmental silicon carbide (SiC) devices measured from Cree, Inc., were a Schottky diode rated 75 A and 1200 V sent on 6 December 2005 and two metal oxide semiconductor (MOS) transistors #32 and #33 rated 5 A and 1200 V received in 2005. Their incremental capacitance C was measured by a quickly rising negative pulse as a function of voltage to 600 V at room temperature. This reverse biased the diode and put a negative pulse to the MOS source with the drain grounded. C was also measured on a gain-phase analyzer as a function of frequency and bias voltage to 40 V. For MOS that has Miller multiplication, adequate speed needs small $C_{\text{drain-source}}$ and for diode a small C_{reverse}. These would help applications such as a three-phase inverting motor drive.

2. Measurement Apparatus

The pulse generator used was Industrial Research, Co., (IRCO, now HV Pulse Technologies, Inc.) model MK25; for fast rise time, it had its proper output cable and a vacuum tube. Its external system ground was connected to a wall outlet's ground. The pulse generator produced only negative output pulses selectable from slightly larger than –1500 V; we used as large –3300 V. A measurement sweep used one manually triggered pulse. Pulse width was selectable from 3 μs to 1000 μs; we chose 740 μs to be long enough for diode V_{reverse} or V_{ds} and V_{series} to stabilize. The pulse generator's load was greater than 10 kΩ to give droop specified <8%/100 μs and observed as an acceptable 2.7%/100 μs. The devices were not encapsulated, so the pulse across the device was limited to -600 V.

Resistors for the voltage divider were chosen as 6.8 kΩ or less to have a sufficiently constant resistance, with reactance an acceptably small fraction of impedance, to above 10 MHz as seen on an HP4194A gain-phase analyzer. The planar (low inductance) resistors series FPA100 from Arco were rated 1 kV and had thermal mass from a metal base 3.7 cm by 2.5 cm by 0.2 cm thick to withstand the pulse energy. Resistors other than R_{gs} were FPA100 and did not feel warm. Both these planar resistors and carbon composite resistor of 2-W above 10 kΩ measured mostly resistive to a frequency increasing at least six times as resistance decreased ten times; for example, a carbon composite 10 kΩ of 2-W at 23 MHz had impedance magnitude 8.22 kΩ with a phase far too large at 45 degrees. Two 5-kΩ ordinary carbon resistors of 1-W in series could withstand the pulse generator's voltage and went from where the pulse generator was being resistively divided to the divided voltage point. That point went to the pulsed end of the capacitance and through an FPA100 with selected resistance to ground. That resistance value

determined the pulse amplitude; a 98-Ω resistor and -1600 V from the pulse generator provided a –16-V pulse. A 663-Ω resistor gave –100 V, a 991-Ω resistor at various pulse generator voltages gave –200 V and –300 V, and a 3186-Ω resistor at various pulse generator voltages gave –400 V, –500 V, and –600 V. The divided voltage's rise time was negligible ~250 ns. The oscilloscope measurement was a single sweep triggered by this rise. Our fall time was slower and not used for measurement.

The other end of the capacitance (opposite the divided voltage point) went through a 26.6-kΩ series resistance to the pulse generator ground. For adequate frequency, this resistance was four 6.7 kΩ FPA100 in series connected by copper strip 0.9 cm wide by 0.08 cm thick. The series resistance was much larger than the resistance from the divided voltage point to ground so the divided voltage was not loaded. The series resistance also limited device current by slowing from less than 1 μs to at least tens of microsecond the capacitance charging, and to a lesser extent, the discharging, which were measured. Some MOS in general have *C* small, so resistors as great as 100 kΩ should be considered for adequate *RC* time constant.

In the schematic in figure 1, a Tektronix TCP312 sliding clamp current probe measured capacitance current accurately from DC to 100 MHz with negligible insertion impedance <0.7 Ω. Another measurement of current was the differential voltage across our series resistors; since they were not a perfectly constant resistance with frequency, this seems less accurate for the zeroing used.

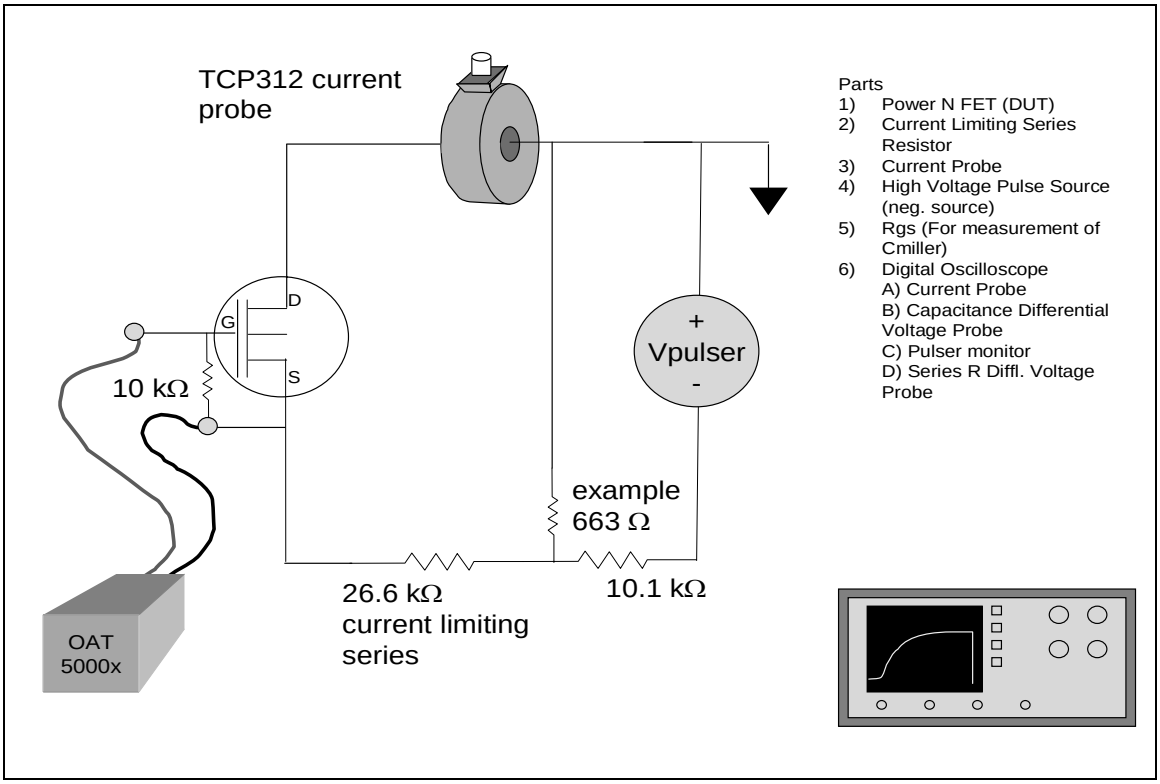


Figure 1. Apparatus.

We did not use doughnut-shaped current monitors Pearson models 4100 and smaller 2877. Each one could measure the current from a sine signal generator into a 50-Ω resistor as specified over its adequate frequency range but in the circuit were inaccurate; the 2877 gave 1/5 of a nearby probe's correct measurement and sometimes much noise. A Rogowski current probe rated 30 A and 6 MHz was for our small currents far too noisy and slow.

Differential voltage probes were Yokogawa model 700924 rated to 100 MHz; impedance 4 MΩ in parallel with 10 pF was neglected. Input divided by 100 was rated ±140 V or pulse ±350 V and was used when possible for better signal-to-noise ratio than input divided by 1000. These attenuations were entered into the oscilloscope scales. They should have been on internal battery power and not from a DC adapter from a wall outlet for less possible offset during the measurements. An OA250 probe was too slow.

The pulse generator manually gave a single pulse, and its synchronous out TTL signal triggered the TDS5104 oscilloscope through its external. The apparatus was proven with a 1-nF mica and a 0.1-nF disc capacitor and a commercial Si MOS IRFPS40N60 rated 40 A. Si MOS V_{gs} across its R_{gs} was initially measured, and representative maximum V_{gs} of 2.8 V was less than the $V_{threshold}$ of 3 V to 5 V. For R_{gs} = 10 kΩ, integration over time of V_{gs}/R_{gs} calculated 1.5 nC of gate charge; this was negligibly smaller than Q_{ds}, and R_{gs} around 1 kΩ gave similar V_{gs} and did not change other curves. Thus, we used 10 kΩ which kept V_{gs} adequately small with decay several times longer than that of current and V_{ds}. For an SiC MOS, we should have for curiosity measured V_{gs}.

The oscilloscope with eight vertical divisions on the screen digitized from –5.12 to 5.12 vertical divisions into 256 levels, which gave artificial steps. The pulse generator brief initial spike gave initial current peaks needing 4- to 10-ns/point measurement and typically 25,000 data points. The oscilloscope's high resolution mode could have been conveniently added for another measurement sweep at each voltage. At a slow enough sweep, this mode resolves more levels for at least 110 MHz bandwidth, which supports the bandwidth of the probes, so it would reduce some random noise and the vertical digitization step size. We did not use the averaging mode at each point over at least several sweeps to reduce random noise; it was not immediately compatible with our triggering from the pulse generator pulse.

From the oscilloscope's data digitized for the TCP312 current, for V_{ds}, and for V_{series}, a moving average of 401 points in time was calculated on a desk computer. The moving averages reduced random noise and the digitization steps; each of these three was zeroed by our only realistic way, subtraction of the average for the untriggered first 1000 points. This gave computational compatibility. At a point we took dV_{ds}/dt as 1/400 times the change of the averaged V_{ds} value from the point 200 points before to the value for 200 points later. When V_{ds} flattened later into the pulse, the dV_{ds}/dt, the current, and particularly the $V_{series}/26600$ became too small and erratic to calculate C and were not used. Total capacitance was also calculated.

We did not assume that the total capacitance was constant from 0 V to the pulse voltage. The voltage exponential rise time constant measured with cursors from 0% to 63% of maximum could thus be divided by R_{series} for the total capacitance.

3. Diode Measurements

The Schottky diode chip rated 75 A and 1200 V was bonded in a package 2.5 cm square. An HP4194A measured the data in table 1.

Table 1. Incremental capacitance *C* of SiC diode at frequency and voltage.

	0 V (nF)	1 V reverse (nF)	10 V reverse (nF)	40 V reverse (nF)
100 Hz	Large	4.06	1.89	0.98
15 kHz	6	4.07	1.90	1.03
30 kHz	5.5	4.07	1.90	1.03
1 MHz	5.57	4.13	1.92	1.04
3 MHz	7.2	4.98	2.08	1.08
4 MHz	9	6.1	2.26	1.13
6 MHz	through 0	17.6, soon 0	2.98	1.28
10 MHz	—	—	through 0	2.27

The decrease of *C* with reverse bias resembled $(V_{reverse} + V_{built\text{-}in})^{-1/2}$ for large reverse bias as the depletion layer widened (the two conductive layers of the capacitor became farther apart). The increase of *C* while frequency increased toward the resonance frequency was approximately as expected. The resonance frequency increased much more slowly with $V_{reverse}$ than $(V_{reverse} + V_{built\text{-}in})^{1/2}$. This is also true of later MOS measurements.

Pulsed *C* results listed total capacitance in the graph title; for the diode are the next seven graphs (see figure 2). This first graph was noisy. *C* decreased with increased reverse bias. *C* increased with frequency as it approached resonance and was not just a capacitance.

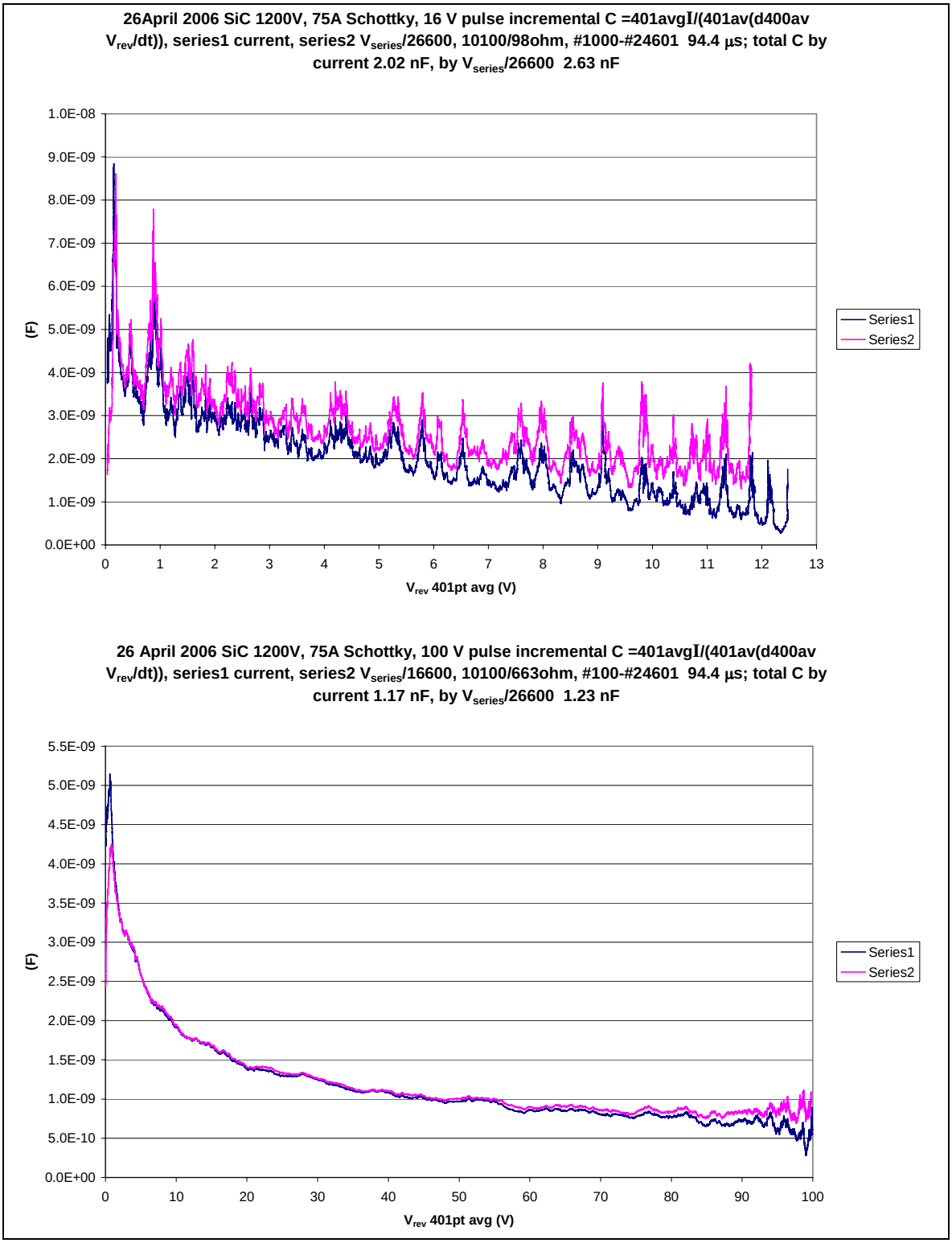


Figure 2. *C* for SiC Schottky diode at pulsed –16 V through –600 V.

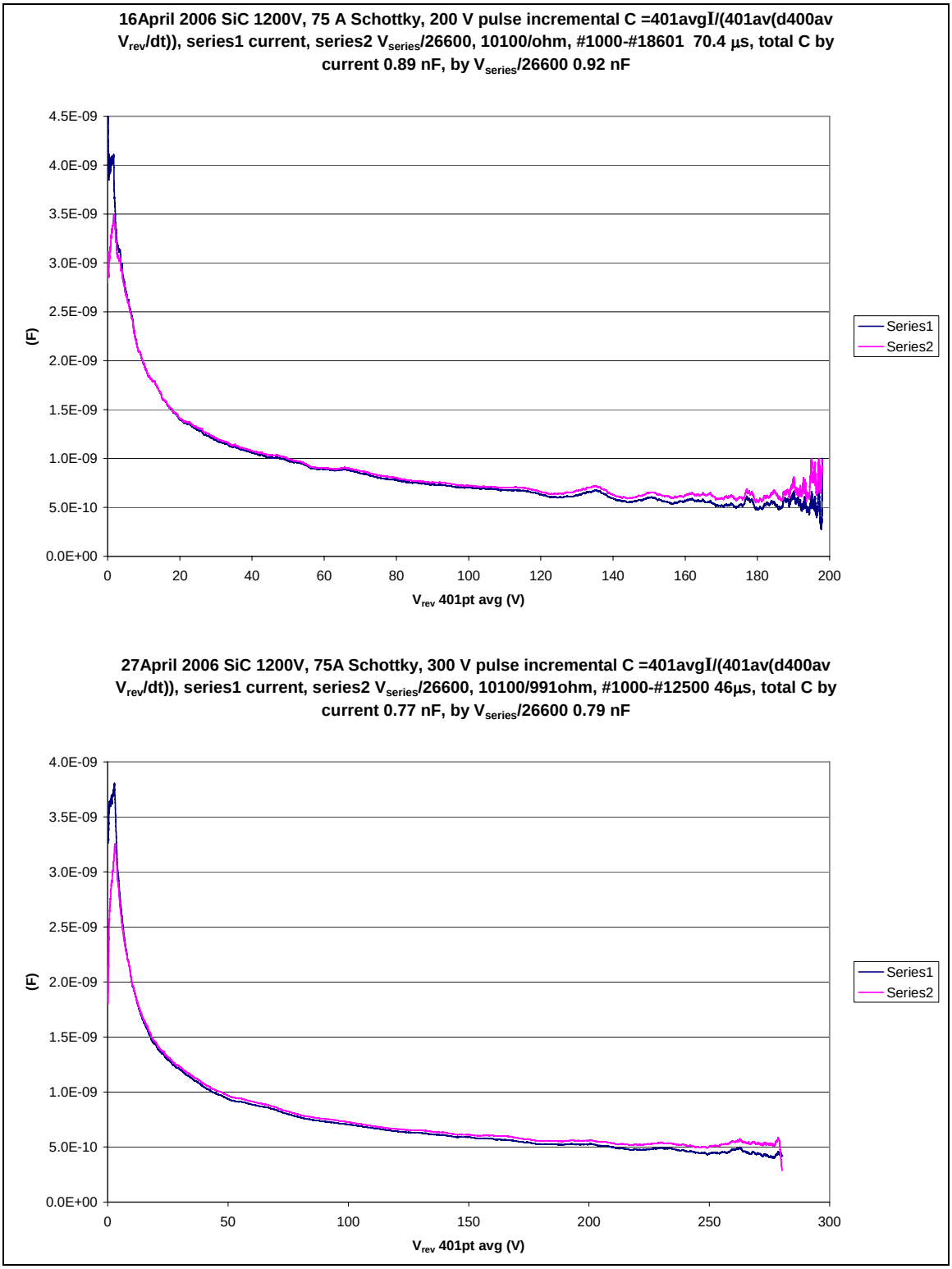


Figure 2. *C* for SiC Schottky diode at pulsed –16 V through –600 V (cont'd).

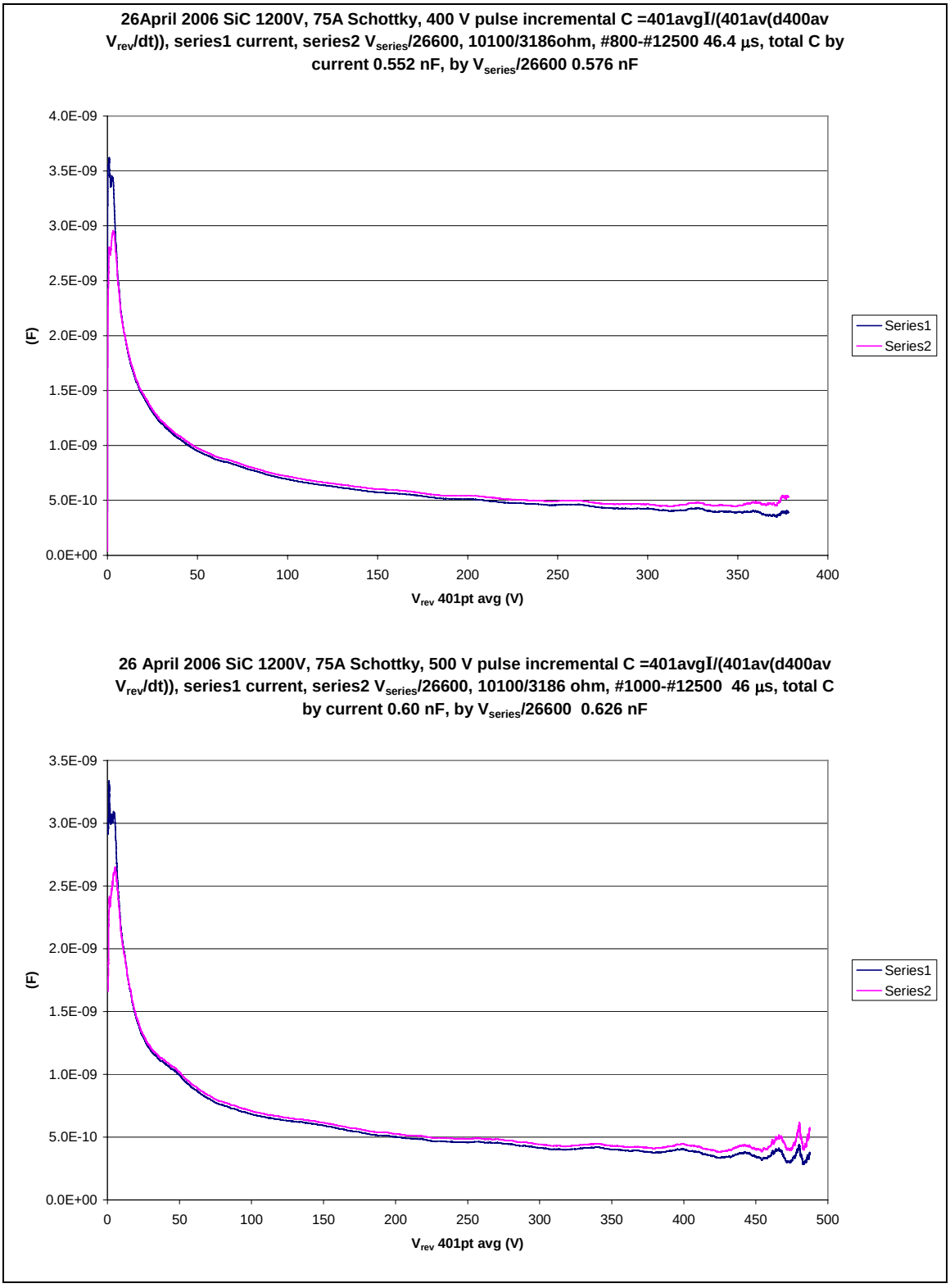


Figure 2. *C* for SiC Schottky diode at pulsed –16 V through –600 V (cont'd).

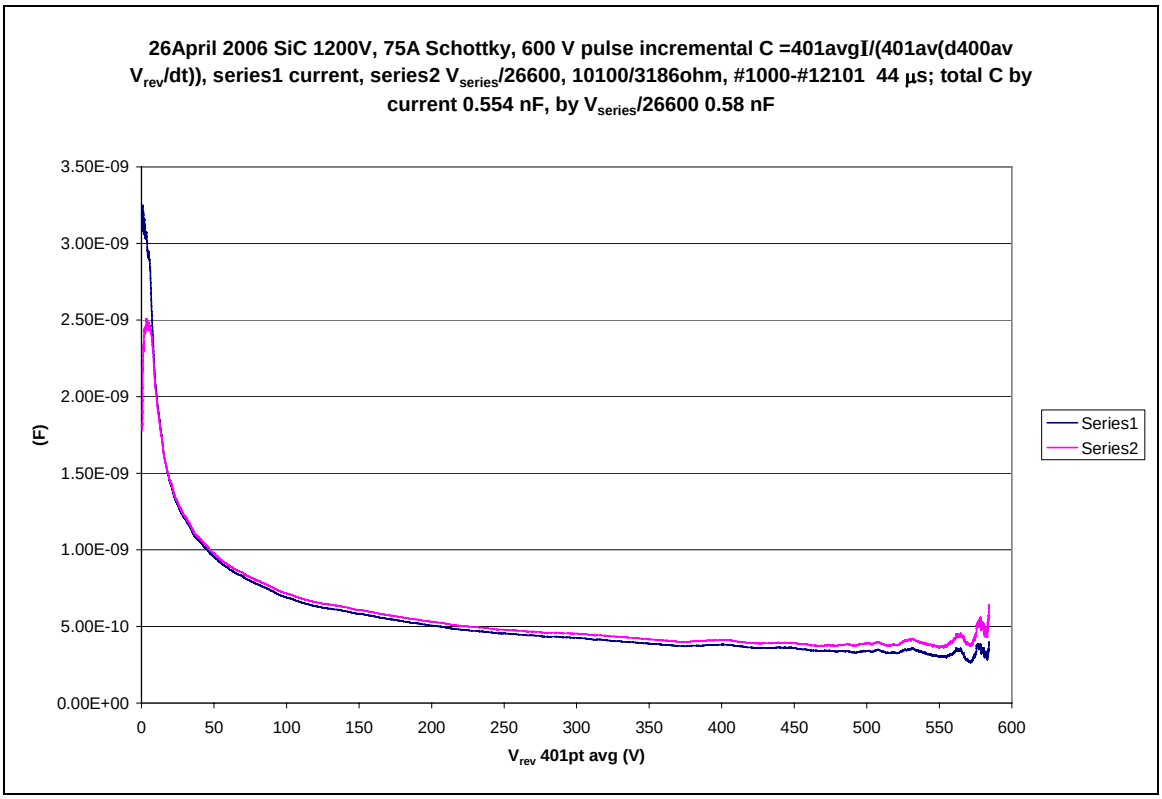


Figure 2. *C* for SiC Schottky diode at pulsed –16 V through –600 V (cont'd).

4. MOS Transistor Measurements

The Si MOS data sheet for $V_{gs} = 0$ at 1 MHz specifies typical $C_{oss} = C_{ds} + C_{gd}$ and the much smaller $C_{rss} = C_{gd}$ as a function of voltage; the difference C_{ds} is large enough to reduce performance, with voltage gain multiplication and the Miller effect for MOS. For comparison to SiC is the data in table 2.

Table 2. Si MOS IRFPS40N60
C_{ds} from data sheet.

V_{ds} (V)	C_{ds} (nF)
1	0.55
8	0.25
10	0.2
14	0.09
20	0.072
100	0.026
200	0.018

The SiC MOS drain was at ground and the source received the negative voltage pulse. Others usually measure with a positive pulse source to the drain, with the gate not having to follow any change in the grounded source voltage. A 10-kΩ resistor between gate and source had for the Si MOS a peak voltage across it of only half the 3 V to 5 V $V_{threshold}$ and only developed V_{gs}/R_{gs} current for a charge much less than the drain-source charge. The MOS were functioning devices for V_{ds} = 0.3 V; MOS #32 at V_{gs} = 7 V had I_D = 20 mA and at V_{gs} = 6 V I_D = 6 mA; MOS #33 had 16.4 mA and 5.1 mA. The HP4194A measured the data in table 3.

Table 3. Incremental capacitance *C* of SiC MOS #32 at frequency and voltage.

	0 V (nF)	1 V reverse (nF)	10 V reverse (nF)	40 V reverse (nF)
100 Hz	2.43 +8 kΩ	1.2 + 7.9 kΩ	0.48	0.268
15 kHz	1.74 +803 Ω	1.06 +491 Ω	0.49 +325 Ω	0.268 +249 Ω
30 kHz	1.68 +295 Ω	1.04 +217 Ω	0.488 +173 Ω	0.266 +169 Ω
1 MHz	1.45 +4.8 Ω	0.941 +5.8 Ω	0.462 + 7 Ω	0.257
3 MHz	1.45	0.927	0.458	0.257
4 MHz	1.46	0.927	0.457	0.257
6 MHz	1.5	0.938	0.459	0.257
10 MHz	1.68	0.993	0.468	0.258
15 MHz	2.27	1.16	0.496	0.264
20 MHz	4.6	1.53	0.543	0.273
23.7 MHz	through 0	2.23	0.60	0.283
29.8 MHz	-	through 0	0.772	0.306
40 MHz	-	-	3.29	0.389

The device total impedance well below 1 MHz and for little reverse bias was mostly series resistance and increased at lower frequency, which had a slowing of the rise in V_{ds} (see figure 3).

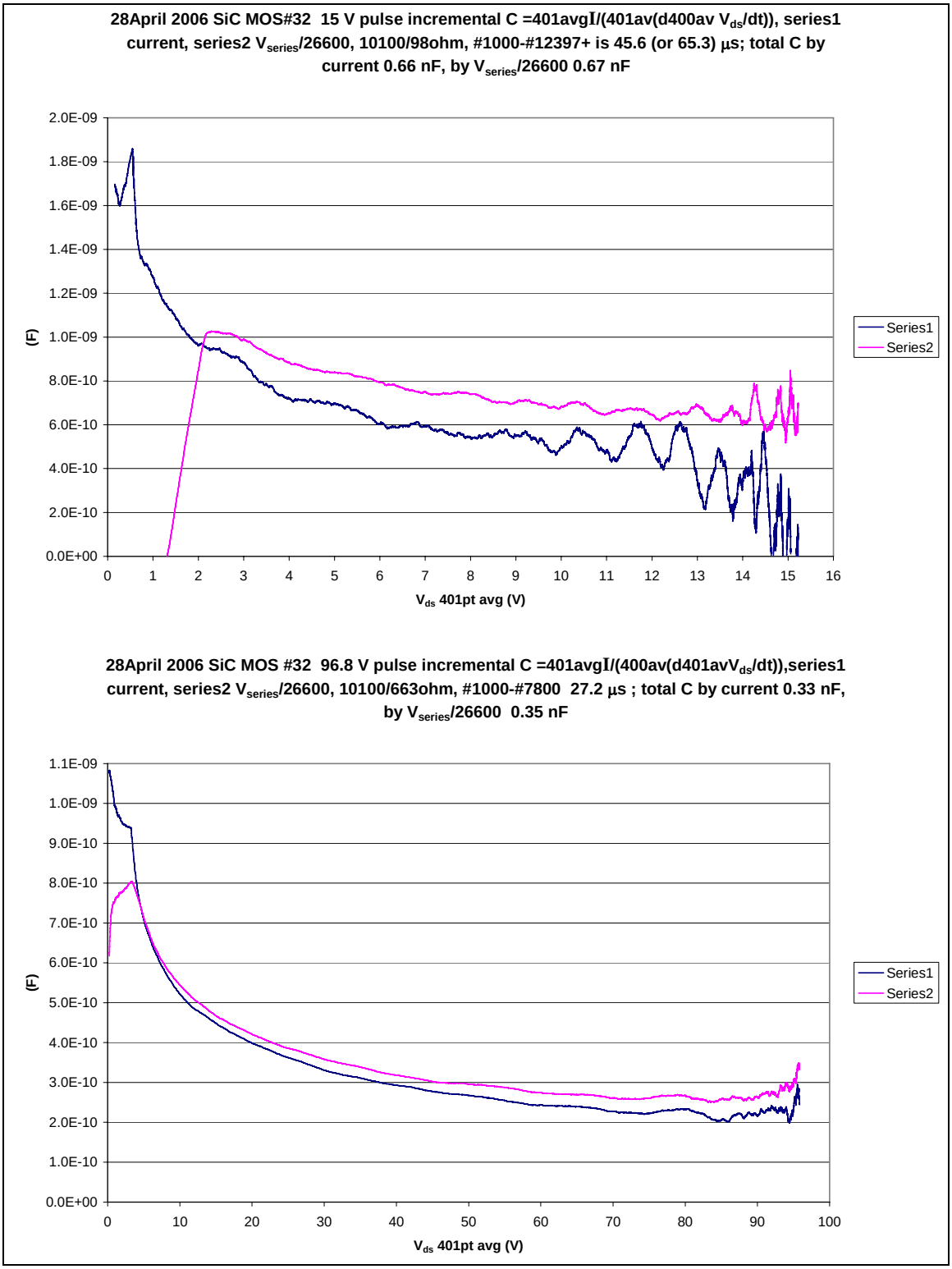


Figure 3. *C* for SiC MOS #32 at pulsed V_{ds} of 15 V through 595 V.

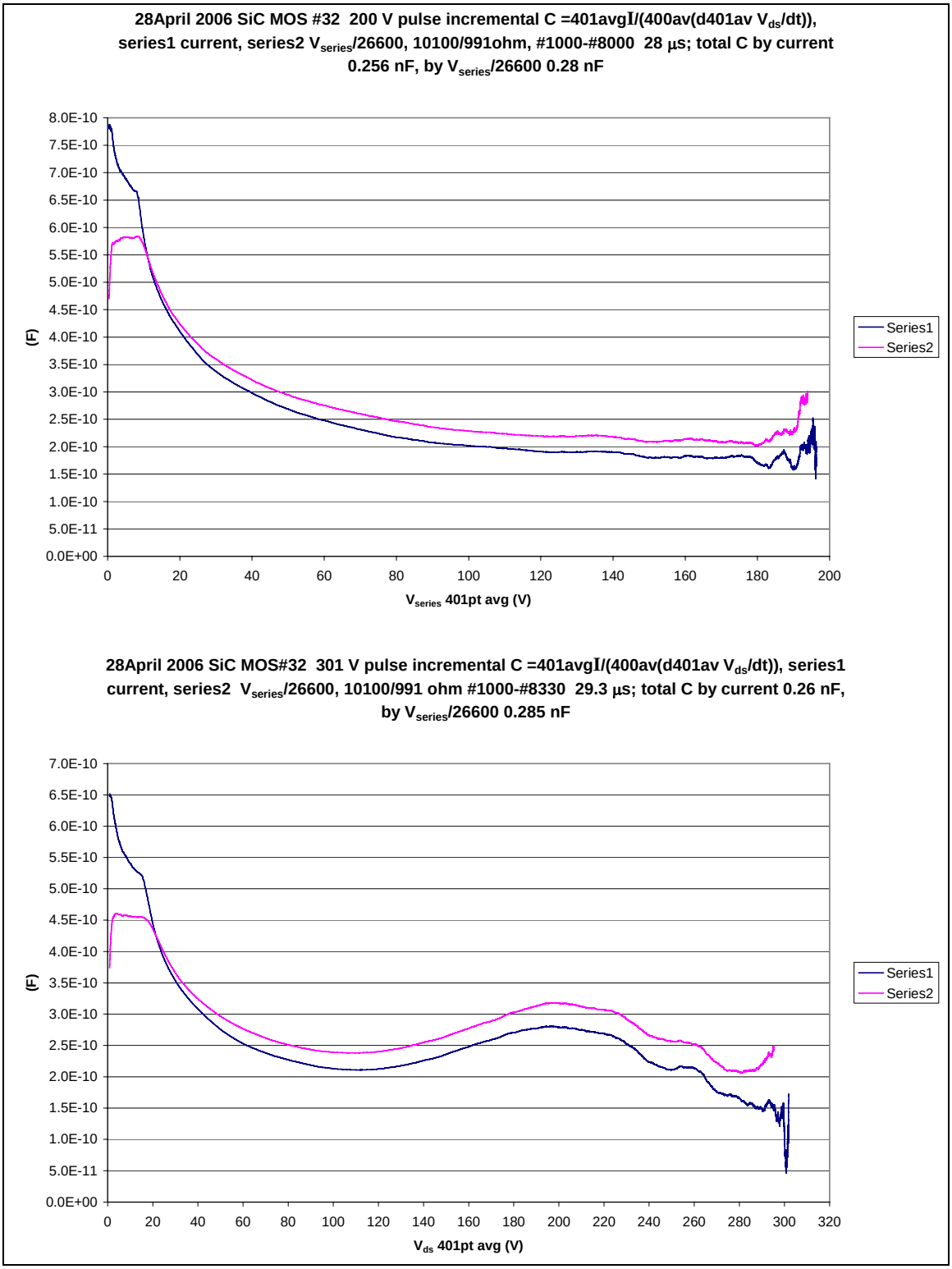


Figure 3. *C* for SiC MOS #32 at pulsed V_{ds} of 15 V through 595 V (cont'd).

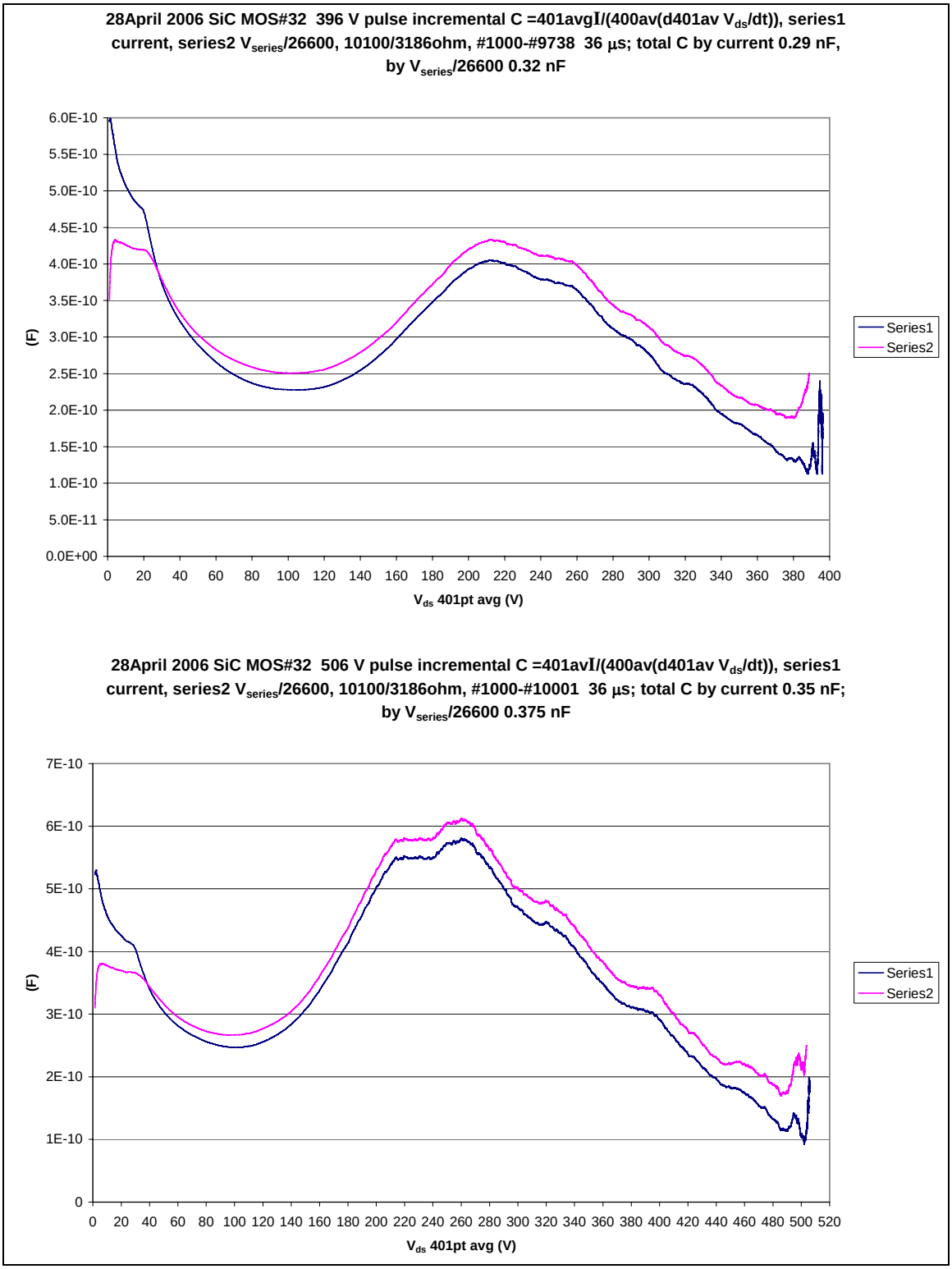


Figure 3. *C* for SiC MOS #32 at pulsed V_{ds} of 15 V through 595 V (cont'd).

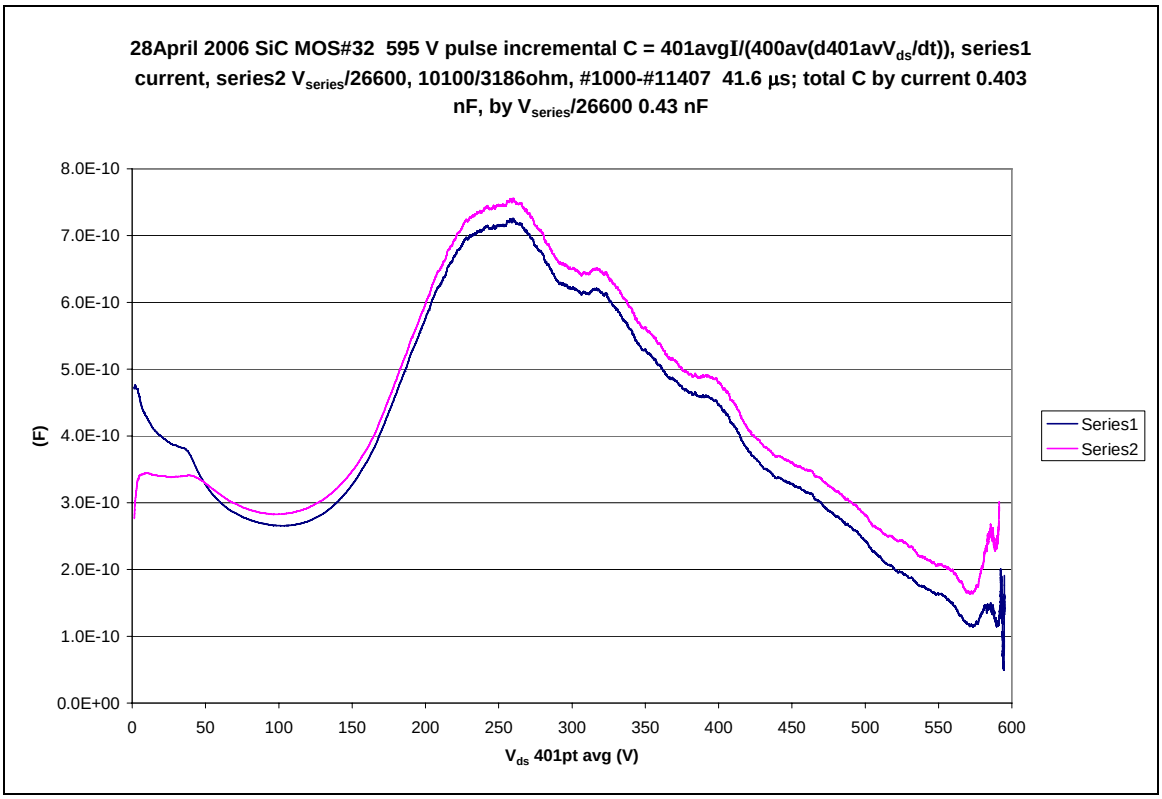
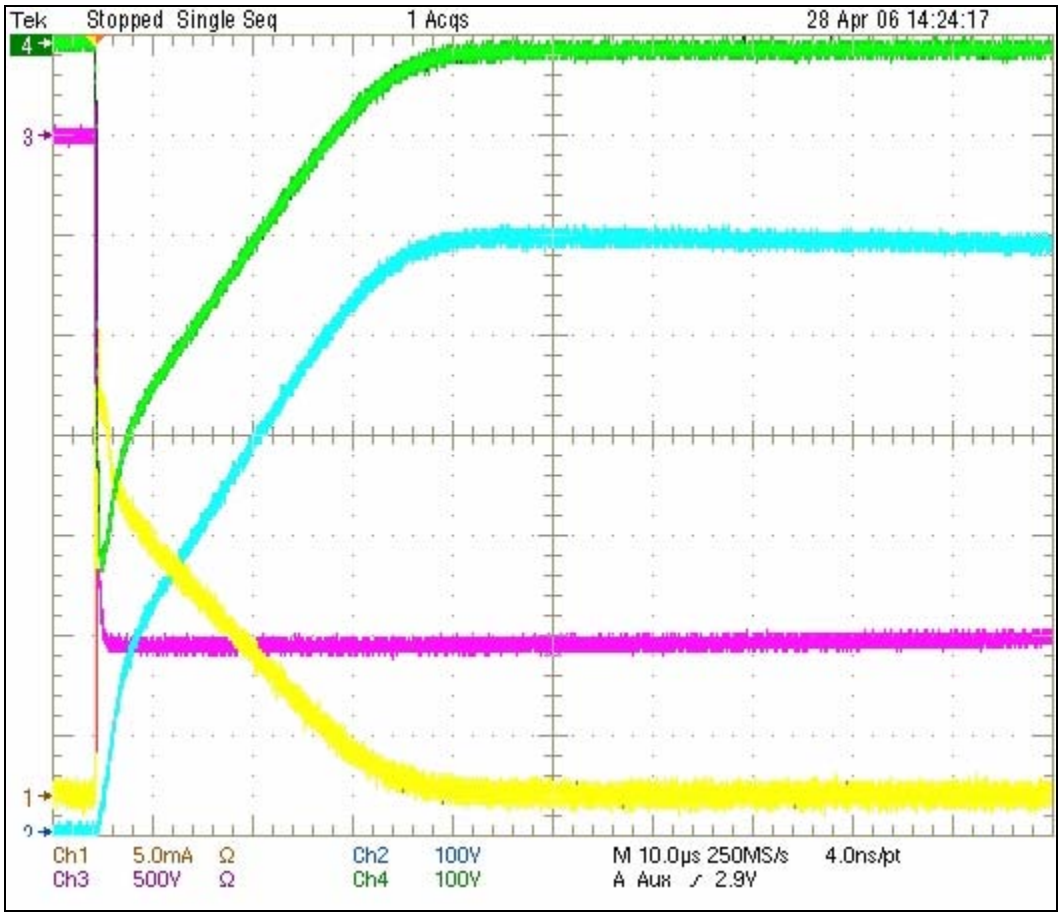


Figure 3. *C* for SiC MOS #32 at pulsed V_{ds} of 15 V through 595 V (cont'd).

In this last graph for MOS #32 to 600 V, for example, the incremental *C* was lower until 160 V, then increased to around 250 V, then more gradually decreased. The graph was calculated from the oscilloscope data in figure 4.



Note: channel 1 capacitive current TCP312; channel 2 V_{ds}; channel 3 pulse generator output; channel 4 $V_{series26600\ ohms}$.

Figure 4. MOS #32 measurement with 600 V pulse.

Channel 2's slope dV_{ds}/dt was correspondingly and definitely reduced above 100 V; with increasing V_{ds}, the slope decreased to a slightly smaller constant value but was definitely non-exponential, then stabilized at 600 V. The V_{ds} rise time from 10% to 90% was 25.4 µs; if we divide by 2.2 for the exponential time constant, this implies that the C was for frequencies on the order of 1/(10.5 µs x 6.28) = 15 kHz. The rapid rise from 10 V to 160 V took 2.8 µs; divided by 2.2 this implied the order of 125 kHz.

Figure 5 is versus time, not voltage. C, labeled series1, first decreased with rapidly higher V_{ds} (labeled series2) to 160 V, then increased while dV_{ds}/dt (thus the frequency) becomes sharply lower after a few microseconds to near 250 V, then gradually decreased with this slowly higher V_{ds}; finally both stabilized.

Results for MOS #33 were close to those of #32. The HP4194A measured the data in table 4.

In the last graph of MOS #33 to 596 V (see figure 6), artificially subtracting 0.5 mA from the realistically zeroed V_{series}/26.6 kΩ mostly fitted its *C* results series 3 to those of the TCP312 current probe.

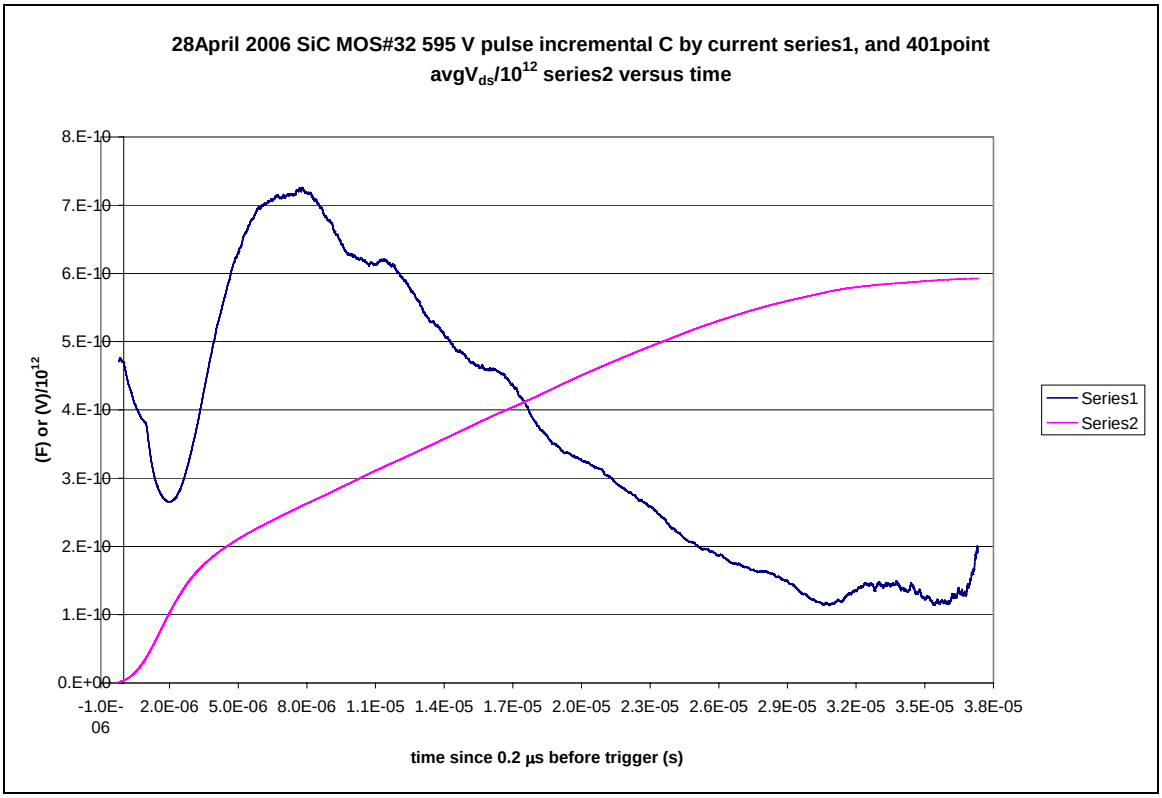


Figure 5. *C* for SiC MOS #32 at 595 V pulse increment.

Table 4. Incremental capacitance *C* of SiC MOS #33 at frequency and voltage.

	0 V (nF)	1 V reverse (nF)	10 V reverse (nF)	40 V reverse (nF)
100 Hz	2.5 +10 kΩ	1.22 +18 kΩ	0.488	0.258
15 kHz	1.8 +830 Ω	1.07 +497 Ω	0.489 +312 Ω	0.267 +226 Ω
30 kHz	1.72 +302 Ω	1.06 +216 Ω	0.487 +169 Ω	0.266 +161 Ω
1 MHz	1.49 +4.5 Ω	0.953 +5.8 Ω	0.462 +6.9 Ω	0.259 +7 Ω
3 MHz	1.49	0.94	0.458	0.258
4 MHz	1.51	0.94	0.457	0.257
6 MHz	1.56	0.955	0.46	0.257
10 MHz	1.8	1.02	0.472	0.259

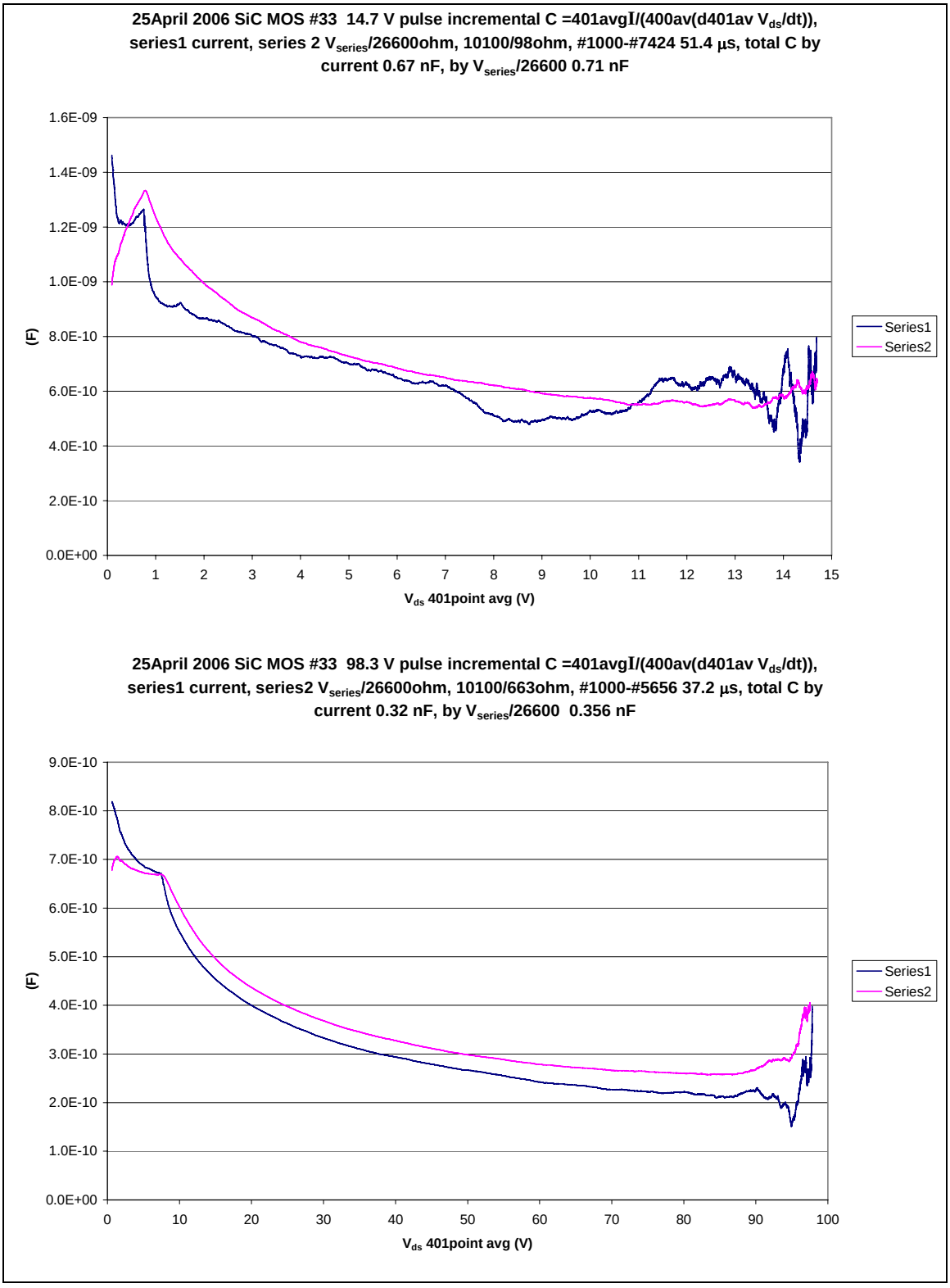


Figure 6. *C* for SiC MOS #33 at pulsed V_{ds} of 14.7 V through 596 V.

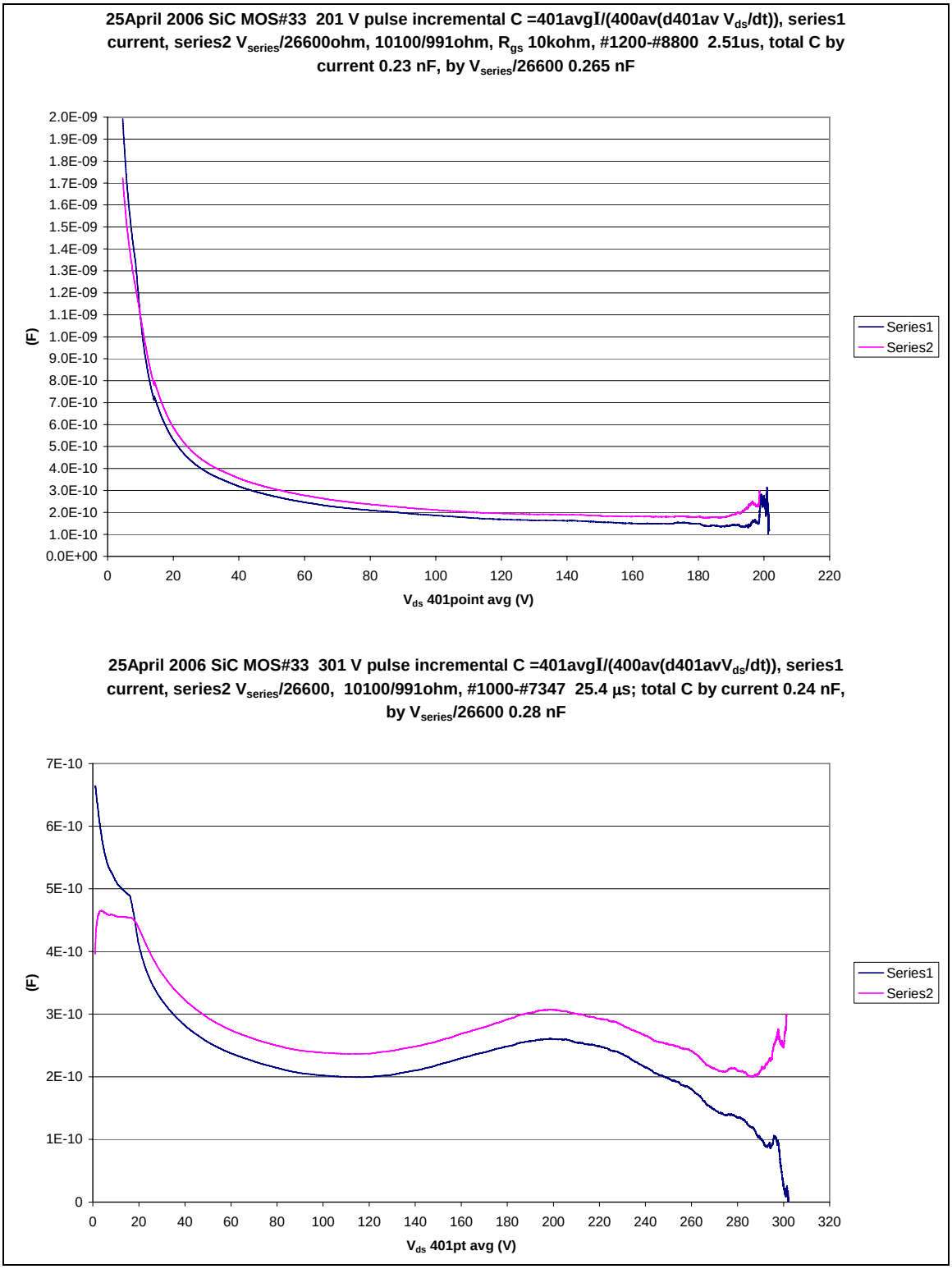


Figure 6. *C* for SiC MOS #33 at pulsed V_{ds} of 14.7 V through 596 V (cont'd).

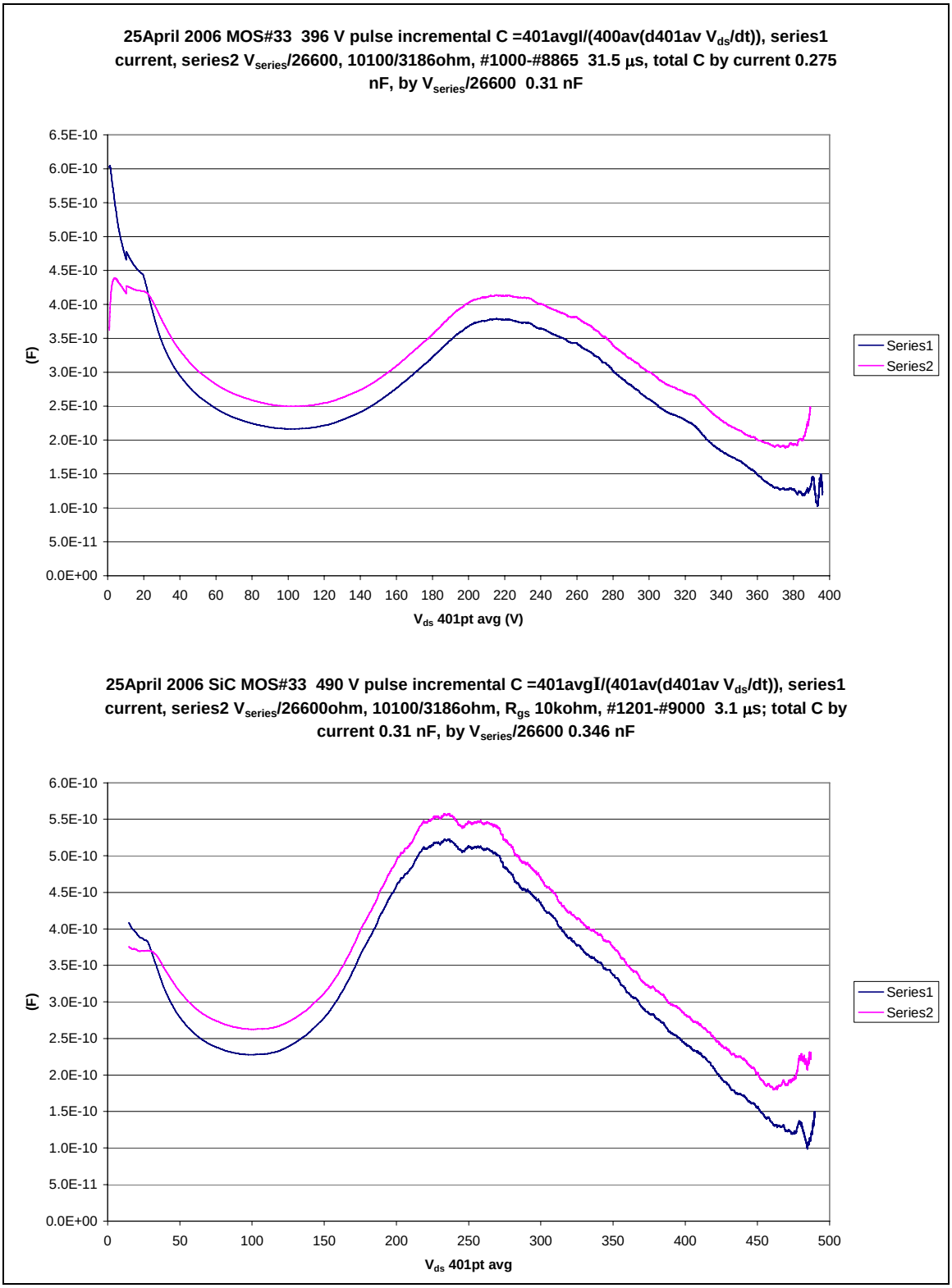


Figure 6. *C* for SiC MOS #33 at pulsed V_{ds} of 14.7 V through 596 V (cont'd).

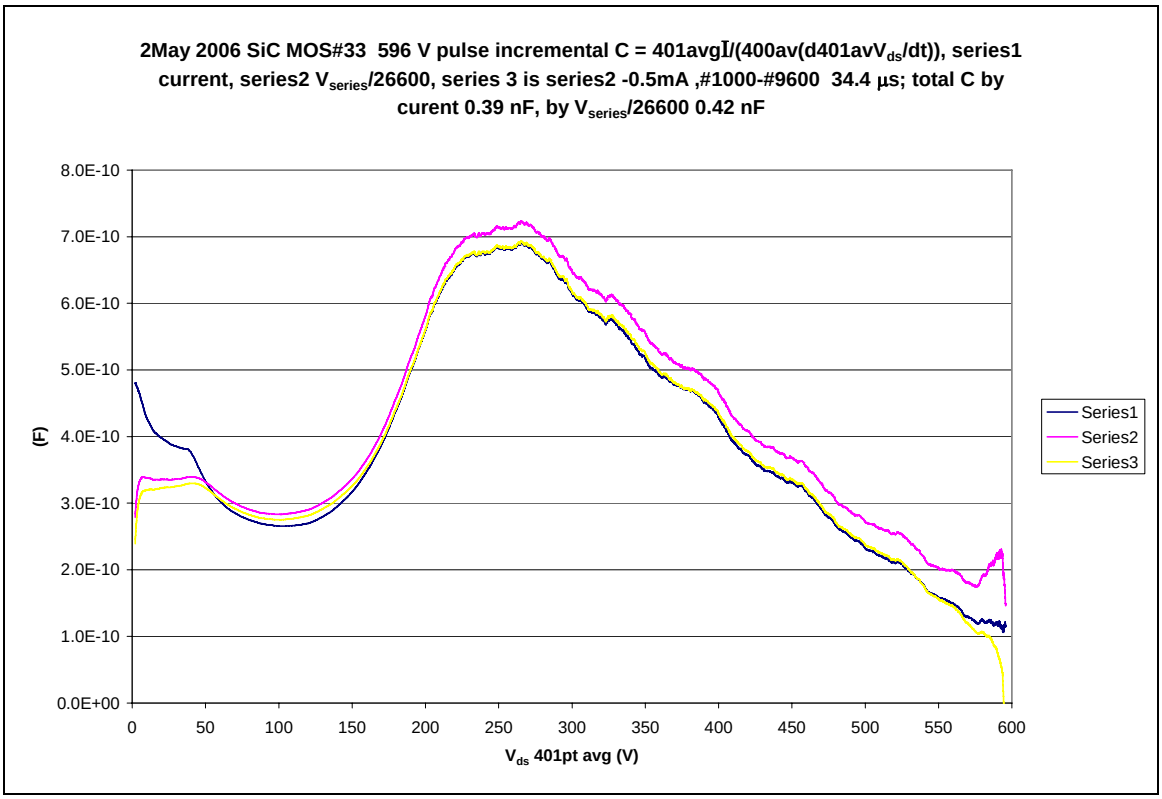


Figure 6. *C* for SiC MOS #33 at pulsed V_{ds} of 14.7 V through 596 V (cont'd).

5. Discussion

Overall, the pulse measurement's total capacitance and incremental C_{ds} as a function of voltage are far from being at one constant effective frequency or constant d*V*/d*t* (see table 5), so these results are less comparable than is 1 MHz with measurements by others. Pulse testing should be more comparable for hard-switched applications. For SiC MOS rated 5 A, the pulse-measured C_{ds} in tables 6 and 7 is seven to eleven times that of the commercial Si MOS rated 40 A. In tables 3 and 4 at 1 MHz the SiC MOS C_{ds} at 1 V is 1.7 times and at 20 V is five times that of the commercial Si MOS. These are not production MOS or as developed and engineered as the larger Si MOS.

Table 5. Diode total capacitance *C* and incremental *C*.

pulse (V)	total capacitance by current (nF)	total capacitance by V/26600 (nF)	*C* near peak V (nF)
16	2.02	2.63	1.5
100	1.17	1.23	0.75
200	0.89	0.92	0.6
300	0.77	0.79	0.5
400	0.552	0.576	0.5
500	0.60	0.626	0.4
600	0.554	0.58	0.3

Table 6. MOS #32 total C_{ds} and incremental C_{ds}.

pulse (V)	total C_{ds} by current (nF)	total C_{ds} by V/26600 (nF)	C_{ds} near peak V (nF)
15	0.66	0.67	0.5
96.8	0.33	0.35	0.25
200	0.256	0.28	0.2
301	0.26	0.285	0.18
396	0.29	0.32	0.16
506	0.35	0.375	0.15
595	0.403	0.43	0.14

Table 7. MOS #33 total C_{ds} and incremental C_{ds}.

pulse (V)	total C_{ds} by current (nF)	total C_{ds} by V/26600 (nF)	C_{ds} near peak V (nF)
14.7	0.67	0.71	0.6
98.3	0.32	0.356	0.24
201	0.23	0.265	0.16
301	0.24	0.28	0.15
396	0.275	0.31	0.16
490	0.31	0.346	0.16
596	0.39	0.42	0.16

A gain-phase analyzer also measured *C* as a function of frequency and bias to 40 V. The decrease of *C* with diode large reverse bias resembled $(V_{reverse} + V_{built\text{-}in})^{-1/2}$ as the depletion layer widened. The increase of *C* for frequency increasing toward the resonance frequency was approximately as expected. The resonance frequency increased much more slowly with $V_{reverse}$ than $(V_{reverse} + V_{built\text{-}in})^{1/2}$.

6. Conclusions

Incremental capacitance C was measured for one SiC Schottky diode by a reverse bias voltage pulse and for two SiC MOS by a negative pulse to the source as a function of voltage to 600 V with the drain grounded; the total capacitance of each was also calculated. For MOS, the increase in C for a slowing of dV_{ds}/dt (a lower frequency) was offset by the decrease in C for larger V_{ds}. Compared to an Si MOS with eight times the current rating, the SiC MOS had a much larger C which should be re-engineered to be smaller for applications.

A gain-phase analyzer measured C as a function of frequency and bias to 40 V. The decrease of C resembled $(V_{reverse} + V_{built\text{-}in})^{-1/2}$ as the depletion layer widened.

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